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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/934,618	08/22/2001	Michael Anh Nguyen	13151.1US01	8664

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EXAMINER	
COURTENAY III, ST JOHN	
ART UNIT	**PAPER NUMBER**
2126	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/934,618	NGUYEN, MICHAEL ANH	
	Examiner	Art Unit	
	St. John Courtenay III	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ST. JOHN COURTENAY III
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-21-2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 10-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Thomas et al.** (U.S. Patent 5,649,001) in view of **Shafe'** (U.S. Patent 5,918,068).

As per independent claims 1, 19:
Thomas discloses the invention substantially as claimed: Thomas teaches an electronic apparatus for operably coupling to at least a first device of a variety of devices having at least one connector thereon, the apparatus comprising:

- a variety of connectors, wherein the variety of connectors include a first connector that connects to the at least one connector [see universal connector means, col. 8, line 14];

- (re: claim 19) the at least one memory includes at least a device driver portion and a connector core portion [see device driver and software routine dynamic configuration according to the connected device, col. 6, lines 21-50].

- a programmable coupler having an input for receiving coupling instructions and having communication ports coupled to the variety of connectors, wherein at least one of the communication ports is coupled to the first connector, the programmable coupler for coupling the at least one communication port in accordance with the coupling

instructions [see communication interface device 20 and associated discussion, col. 8, beginning line 14];

- a controller coupled to the programmable coupler, the controller for determining that the first device is connected to the first connector, and for providing the coupling instructions, the controller for accessing a first device driver of a variety of device drivers, and accessing a first connector core of a variety of connector cores, and the controller being coupled to provide the first device driver [col. 6, line 29] and the first connector core [see "hardware to detect when a communication adapter cable is connected to or removed from the universal adapter cable, col. 6, lines 51-64; see also function of communication interface that detects when an adapter cable is connected or removed, discussion col. 11, beginning line 1]; and

- receiving the first device driver and the first connector core, for configuring at least some of the variety of logic resources in accordance with the first connector core to provide a first connector processor and first device driver and the, and for configuring the first device driver to operate with the connector processor, wherein the first device driver and the first connector processor establish communication with the first device via the programmable coupler [see device driver and software routine dynamic configuration according to the connected device, col. 6, lines 21-50].

However, **Thomas** does not *explicitly* teach the following additional limitations:

Shafe teaches the use of a programmable logic unit, as claimed [e.g, see Shafe "PLU 24" and associated discussion beginning, col. 5, line 19; see also col. 6, line 51].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by **Thomas** by implementing the improvements detailed above because it would provide **Thomas's** system with the enhanced capability of "dynamic programming of the interface" [e.g., see **Shafe**, col. 5, line 40].

As per independent claim 29:
This claim is rejected for the same reasons detailed above in the rejection of independent claim 1, and also for the following additional reasons:

Thomas, as modified by **Shafe**, teaches a method in a reconfigurable communication interface for operably coupling to a first device of a variety of devices, the first device having at least one connector thereon, the method comprising the steps of:

a) providing the reconfigurable communication interface comprising: a variety of connectors, wherein the variety of connectors include a first connector that connects to the at least one connector [see universal connector means, col. 8, line 14]; a programmable logic device having a plurality of communication ports coupled to the variety of connectors; and a controller coupled to the programmable logic device [e.g, see Shafe "PLU 24" and associated discussion beginning, col. 5, line 19; see also col. 6, line 51];

b) detecting the first device is physically connected to the fist connector [see detection discussion col. 5, lines 19-21];

c) accessing a first connector core of a variety of connector cores associated with the first connector [e.g., see Thomas "Communication adapter cable 22" and associated discussion col. 8, beginning line 60];

d) configuring a first connector processor in the programmable logic device [e.g, see Shafe "PLU 24" and associated discussion beginning, col. 5, line 19; see also col. 6, line 51];

e) accessing a first device driver of a variety of device drivers associated with the first device [see Thomas discussion, beginning col. 6, line 29].

f) configuring the first device to operate with the first connector processor in the programmable logic device [e.g, see Shafe "PLU 24" and associated discussion beginning, col. 5, line 19; see also col. 6, line 51]; and

g) establishing communication with the first device through the first connector using the first connector processor and the first device driver [e.g., see Thomas "communication interface device 20" and associated discussion col. 8, beginning line 14].

As per dependent claim 2:
Thomas teaches a memory having at least another connector thereon, wherein the variety of connectors include a second connector that couples to the at least another connector, the memory having at least a device driver portion and a connector core portion [see device driver and software routine dynamic configuration according to the connected device, col. 6, lines 21-50].

As per dependent claims 3, 4:
Thomas teaches the use of a semiconductor memory comprising one or more random access memory, dynamic random access memory, read only memory, programmable read only memory [see RAM, ROM, PROM, col. 10, line 31; see EEPROM, col. 13, line 36].

As per dependent claims 5, 6:
Shafe teaches where the magnetic memory comprises a hard disk drive [see component disk drive 21, fig. 1 and associated discussion, col. 3, line 65].

As per dependent claim 7:
Shafe teaches second connector and the at least another connector comprises matching IDE connectors [see use of IDE bus, col. 9, line 8; see IDE interface col. 9, line 44].

As per dependent claims 10, 11:
Shafe teaches the controller comprises at least one microprocessor coupled to a memory [col. 10, lines 3-4; see RAM memory 52, col. 10, line 8; see Shafer, SRAM, EEPROM, flash memory, col. 5, lines 42, 43 and Intel 80186 16 bit controller col. 5, line 41].

As per dependent claim 12:
Thomas teaches the at least one memory includes at least a device driver portion and a connector core portion [see device driver and software routine dynamic configuration according to the connected device, col. 6, lines 21-50].

As per dependent claims 13 -16:
Shafe teaches the programmable coupler comprises at least one matrix switching device, multiplexer, a programmable logic device, a programmable logic array, or a field programable gate

array [e.g, see "PLU 24" and associated discussion beginning, col. 5, line 19; see also col. 6, line 51].

As per dependent claim 17:
Thomas teaches the variety of connectors comprise a plurality of at least one of the variety of connectors [see universal connector means, col. 8, line 14].

As per dependent claim 18:
Shafe teaches the variety of connectors includes one or more of the following connectors: an IDE connector, a USB connector, an audio connector, a video connector, a serial connector, a parallel connector, a Firewire connector, a PCI connector and a PCMCIA connector [see use of IDE bus, col. 9, line 8; see IDE interface col. 9, line 44].

As per dependent claim 20:
Thomas teaches the first memory further comprises an application portion for storing a variety of application programs that operate with at least some of the variety of device drivers and some of the variety of connector cores to support the exchange of services with at least some of the variety of devices [see communication interface discussion col. 6, lines 21-49].

As per dependent claim 21:
Thomas teaches the first memory further comprises an operating system portion and a program portion [col. 6, lines 21-50].

As per dependent claim 22:
Thomas teaches the program portion includes a main program portion [inherent in the communication interface device], an initialization program portion [col. 6, lines 24-36] and a power down program portion [see sleep or low power mode, col. 6, line 62; also col. 4, line 52].

As per dependent claim 23:
Shafe teaches a second memory coupled to the controller and coupled to the programmable logic device, the second memory for providing working storage for the controller and/or the programmable logic device [see Shafer, SRAM, EEPROM, flash memory, col. 5, lines 42, 43].

As per dependent claim 24:
Shafe teaches the controller comprises a microcontroller [see 80186 16-bit controller, col. 5, line 41].

As per dependent claims 25 & 26:
See the rejections of claims 3 & 4 detailed above. See also Shafer, SRAM, EEPROM, flash memory, col. 5, lines 42, 43

As per dependent claim 27:
See the rejections of claims 13-16 detailed above.

As per dependent claim 28:
See the rejection of claim 18 detailed above.

As per dependent claim 30:
Thomas teaches dynamic configuration and detection of a variety of devices and associated connectors, as claimed [e.g., see "reconfigurable communication interface device" and associated discussion col. 5, beginning line 20].

As per dependent claim 31:
See the rejection of claim 22 detailed above.

As per dependent claim 32:
Thomas teaches the step of detecting whether a first communication port of the plurality of communication ports, which is coupled to the first connector, is active [see sleep or low

power mode, col. 6, line 62; also col. 4, line 52].

As per dependent claim 33:
Thomas teaches detecting whether the first communication port is active comprises detecting the status of one or more signals associated with the first communication port [see sleep or low power mode, col. 6, line 62; also col. 4, line 52].

Claims 8 & 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Thomas et al.** (U.S. Patent 5,649,001) in view of **Shafe'** (U.S. Patent 5,918,068), and further in view of **Hirono et al.** (U.S. Patent 6,633,531).

As per dependent claims 8 & 9:
Thomas, as modified by **Shafe**, discloses the invention substantially as claimed, as discussed above.

However, **Thomas & Shafe** do not *explicitly* teach the following additional limitations:

Hirono teaches the notoriously well known use of an optical memory i.e., a read/write optical disk drive as claimed. [e.g, see discussion col. 4, beginning, line 20].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by **Thomas & Shafe** by implementing the improvements detailed above because it would provide the system of **Thomas & Shafe** with the enhanced capability of a persistent storage medium with a larger storage capacity per disk than magnetic storage devices.

Prior Art not relied upon:
Please refer to the references listed on the attached PTO-892 which are not relied upon in the claim rejections detailed above.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to St. John Courtenay III, whose telephone number is 571-272-3761. A voice mail service is also available at this number. The Examiner can normally be reached on Monday - Friday, 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-AI who can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses sent by U.S. Mail should be mailed to:

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http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/faxnotice.pdf

Effective Oct. 15, 2003, ALL patent application correspondence transmitted by FAX must be directed to the new PTO central FAX number:

NEW PTO CENTRAL FAX NUMBER:

703-872-9306

- Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: (703) 305-3900.**

Please direct inquiries regarding fees, paper matching, and other issues not involving the Examiner to:
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The Manual of Patent Examining Procedure (MPEP) is available online at:
http://www.uspto.gov/web/offices/pac/mpep/index.html

ST. JOHN COURTENAY III
PRIMARY EXAMINER